What is Claimed is:

1. A digital system comprising a microprocessor having an instruction execution pipeline with a plurality of pipeline phases, wherein the microprocessor comprises:

program fetch circuitry operable to perform a first portion of the plurality of pipeline phases;

instruction decode circuitry connected to receive fetched instructions from the program fetch circuitry, the instruction decode circuitry operable to perform a second portion of the plurality of pipeline phases; and

at least a first functional unit connected to receive a plurality of control signals from the instruction decode circuitry, the functional unit operable to perform a third portion of the plurality of pipeline phases, the third portion being execution phases, wherein the first functional unit comprises:

first test circuitry connected to receive an operand from a selected test register, and having an output for indicating a condition of the operand;

decrement circuitry connected to receive the operand from the selected test register, and having an output connected to provide a decremented value of the operand to the test register;

adder circuitry connected to receive a program counter value and a displacement value, and having an output connected to conditionally provide a branch address to a program counter register; and

wherein the first test circuitry, the decrement circuitry, and the adder circuitry are all operable to test the operand, decrement the operand, and conditionally provide a branch address to the program counter in response to a single instruction of a first type.

2. The digital system of Claim 1, wherein the first test circuitry, the decrement circuitry, and the adder circuitry are all operable to test the

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operand, decrement the operand, and conditionally provide a branch address to the program counter in response to a single instruction during a single one of the third portion of pipeline phases.

3. The digital system of Claim 1, wherein the first test circuitry is operable to inhibit the program counter from receiving the branch address if the operand has a value that does not correspond to a first condition.

4. The digital system of Claim 3, further comprising second test circuitry connected to test a condition of a selected predicate register, and having an output for indicating a condition of the predicate register, wherein the second test circuitry is operable to inhibit the program counter from receiving the branch address if the contents of the predicate register do not correspond to a second condition.

5. The digital system of Claim 4, wherein the program counter is operable to receive the branch address from the adder circuitry only when the contents of the test register correspond to the first condition and the contents of the predicate register correspond to the second condition.

6. The digital system of Claim 1, wherein the instruction of a first type has a field for identifying the test register and a field to provide the displacement value.

7. The digital system of Claim 6, wherein the instruction of a first type has a field for identifying the predicate register.

8. The digital system of Claim 7, wherein the test register and the predicate register are both part of a same register file.

9. The digital system of Claim 1 being a cellular telephone, further comprising:

an integrated keyboard connected to the CPU via a keyboard adapter;

a display, connected to the CPU via a display adapter;

radio frequency (RF) circuitry connected to the CPU; and

an aerial connected to the RF circuitry.

10. A method of operating a digital system having a microprocessor with a conditional branch instruction, comprising the steps of:

fetching a conditional branch instruction for execution;

testing a test register selected by the conditional branch instruction to determine if the contents of the test register meet a first condition;

providing a branch address to a program counter to cause a branch if the contents of the test register meet the first condition; and

modifying the contents of the test register.

11. The method of Claim 10, further comprising the steps of:

testing a predicate register selected by the conditional branch instruction to determine if the contents of the predicate register meet a second condition; and

inhibiting the step of providing a branch address to the program counter if the contents of the predicate register do not meet the second condition.

12. The method of Claim 10, wherein the step of modifying decrements the test register.

13. The method of Claim 10, wherein the steps of testing, providing, and modifying are all performed during a same execution phase of the microprocessor.

14. The method of Claim 10, wherein the step of modifying is inhibited if the contents of the test register do not meet the first condition.

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